BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

13/Kladar. Thereon 10-5-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. Of: MATSUDA

Serial No.: 09/222,524

Filed: December 18, 1998

For: SEMICONDUCTOR DEVICE

Group: 2811

Examiner: N. Parekh DOCKET: NEC N98039

Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231

DECLARATION UNDER 37 CFR 1.131 OF PRIOR INVENTION IN A WTO MEMBER COUNTRY TO OVERCOME A CITED PATENT REFERENCE

Dear Sir:

The undersigned, being the named inventor of the subject application, declares and states the following:

(1) I conceived of and completed the invention described and claimed in the subject application, in Japan, prior to December 1, 1997, the filing date of the Higgins U.S. Patent 6,064,114 cited in the Office Action mailed June 26, 2001 in the above matter.

(2) As proof thereof, I provide the following::

(a) Exhibit A, which is a full and complete copy of a written Idea Proposal dated prior to September 1, 1997, which I prepared and submitted to the Intellectual Property Division of NEC Corporation, where the document was stored in the "UNIPAT" data base of NEC Corporation. As can be seen, the basic concept of the invention, and drawing thereof, are found in Exhibit A. A sworn English translation of Exhibit A is also enclosed herewith.

(b) My Idea Proposal was accepted for filing, and my written Idea Proposal (Exhibit A) was then supplied to an outside Japanese Patent Law Firm, who then prepared the

HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C.
175 CANAL STREET
MANCHESTER, NH
03101-2335 U.S.A.

603-668-1400

documents for filing a Japanese patent application. The application was prepared, reviewed by me, and filed in the Japanese Patent Office, as Japanese Patent Application Serial No. 359478/1997, filed December 26, 1997.

(3) The foregoing and attachments clearly show a date of conception and completion of the invention of this application all prior to the December 1, 1997 filing date of the Higgins patent. Moreover, having conceived of the invention prior to December 1, 1997, I proceeded diligently to prepare a complete written disclosure of same and to then promptly file a patent application, initially in Japan, and thereafter in the United States, covering the invention. At no time between my conception of the invention, and my filing of the subject U.S. Patent Application, did I ever intend to abandon the invention.

As the named inventor, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Shuichi Matsuda 松田

Shuichi MATSUDA

Date September 14, 2001

AYES, SOLOWAY,
NESSEY, GROSSMAN
& HAGE, P.C.
8 CANAL STREET
ANCHESTER, NH
3101-2335 U.S.A.

603-668-1400

12/ Translation Bureau 10-5-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re US Appln of: MATSUDA

U.S. Application Serial No.: 09/222,524

For: SEMICONDUCTOR DEVICE

VERIFICATION OF TRANSLATION

Assistant Commissioner of Patents & Trademarks
Washington, DC 20231

Dear Sire:

The undersigned hereby certifies that I am conversant in both Japanese and English languages, that I have prepared the attached English translation of the Japanese text attached as Exhibit A, and that the English translation is a true, faithful and accurate translation of the attached Exhibit A.

I further declare that all statements made of my own knowledge are true and that all statements made on information and belief are with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC § 1001, and that such false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date September 1, 2001 Signature Yukuo Nishimura

Typed Name YUKUO NISHIMURA

Address c/o Nishimura International Patent Office Nakamura The First Bldg.
4-2-6, Kitaurawa, Saitama, Saitama, Japan

アイデア提案書

事業部整理番号：753-10074

提案日：1997年 9月 29日

グループコード：

部内番号：1014

[承認欄] 部長： 課長： 主任：

半導技受付日：

[提案者記入欄]

提案者所属：半高実技本・実装技術開発部　　連絡先 TEL：24-24121

提案者氏名：松田　修一　　社員番号：0848104

適用・応用分野：半導体ＩＣのパッケージング

適用製品名：ＣＳＰ　　売上規模：１０８０（百万円／年）

実験・試作状況：○実験・試作完了 ●実験・試作中 ○実験・試作予定あり ○実験・試作予定なし

先行特許調査（調査した中で近い特許公開番号）：なし

先行文献調査（調査した中で近い特許公開番号）：なし

関連提案・特許：

社外発表予定：○無 ●有（何時：　年　月　日、何処で　）

[上司記入欄]

上司氏名：中島宏文

実施見込み：●実施決定 ○可能性有り（２年以内） ○可能性有り（４年以内）

○不明 ○見込みなし（理由：　）

外国出願希望：○無 ●有（国名：米国　）

コメント：

[発明相談コメント欄]

センター担当：　　年　月　日

[評価委員会記入欄]

評価責任者氏名：森重幸夫，菅原健二

決定日：１９９７年１０月３日

評価結果：1. 出願希望 ●コンカレント ○S級 ○通常扱い 2. 公開技報 3. 中止 4. 再検討

外国出願希望：○無 ●有（国名 米国　）

コメント：

センターへの要望：

[署名捺印]

本提案書（図面を含む）の第１ページから第[illegible]ページを読んで発明内容を理解しました。

氏名：　　１９９７年９月２９日

[発明者署名欄]

氏名：松田修一　　１９９７年９月２９日

氏名：　　１９　年　月　日

本文第１ページ目

整理番号：753-10074 本文頁 2／4

1.【発明の名称】

半導体ＩＣ装置の組立方法

（多重配線化による接合部オープン不良低減方法）

2.【発明の特徴】

キャリアテープと半導体チップをキャリアテープに形成された接合電極をチップの電極に接合する工法を取るチップサイズパッケージにおいて、単一の配線に対して半導体チップの電極を複数設け、結線し、キャリアテープ側も一つの配線に対してチップ電極に対応した接合部を複数設けておく、これを接合することで一つの配線に対してキャリアテープと半導体チップの接合部は複数の経路を持つことになる。チップサイズパッケージの組立に於いて電気的な不良が起こりやすいのは接合部のオープン不良に起因する事が多い。接合部の経路を複数とすることでオープン不良の発生率を低減することができる。

3．1［発明の構成と動作、製法と手順等］

特に電源線／グランド線に対して、それぞれの単一配線に対してチップ電極を複数とする。それに対応してキャリアテープの接合電極も複数個設ける。これを各々接合することで対策された単一配線はチップとテープの接合部において複数の伝送経路を持つことになる。

3．2［発明の主な効果］

特に不良が起こりやすい接合部において多重配線化する事でオープン不良を著しく低減することができる。また、複数配線化する場所はグランド電源線でありこれらはチップのコーナー部に配置されることが多い。コーナー部はチップとキャリアテープの熱膨張差が最も累積する場所なのでこれらの箇所に接合部が増えることで相互に力学的に強度を補強し合い、接合不良を低減することができる。

3．3［上記効果が得られる理由］

接合部の配線を多重化することでその内の一つの経路がオープン不良をおこしも他の経路で導通を得ることができる。また、近隣の接合部同士で補強し合うことでキャリアテープとチップの熱病歪差に耐えることができる。

整理番号：753-10074 本文第3/4頁

4．【発明の実施例】

発明の実施例を図にしめす。チップサイズパッケージの組立においてグランド配線に対応するラインをテープ側とチップ側で複数化し各々を接合している。

4－1【実施例の構成】

キャリアテープとチップから成る接合部においてテープの従来配線に対して、同電位に追加配線を設ける。チップにも従来パッドに対して同電位の追加パッドを設け各々を接合する。

4－2【実施例の動作の説明】

単一の配線に対して接合部は2つの経路を持つことになるので一方がオープン不良となってもパッケージの外部ピンは不良とならない。結果としてオープン不良率を著しく低減することができる。

4－3【発明の他の実施例】

単一の配線に対して配線を追加し、接合部を3つの経路にすることでにすることでさらにオープン不良率を低減することができる。

5．1［従来の構成と動作、製法と手順等］

従来は単一の配線に対してチップに単一の接合電極を用意し、キャリアテープにそれに対応した電極を用意しそれを超音波を印可した熱圧着接合にて接合してチップからパッケージに電気的導通を取っていた。このような接合部では接合不良が生じる可能性があり、不良はO／S検査工程や選別工程により不良品として除外することができた。

5．2［従来の主な欠点］

電源線、及びグランド線は複数本の配線により機能しており、それぞれ同電位なので例えばグランド線が10ピンあって1ピンがオープン不良であっても現行のO／S検査工程や選別工程では検出する事ができなかった。この不良は単ピン毎に電気検査すれば検出されるため顧客からのクレーム対象となった。

5．3［上記欠点を生じる理由］

現行の検査工程は同電位の電源線、グランド線をまとめて検査するため、単一のオープンは検出できないため、単一のオープンは検出できないため。

6．【権利範囲】

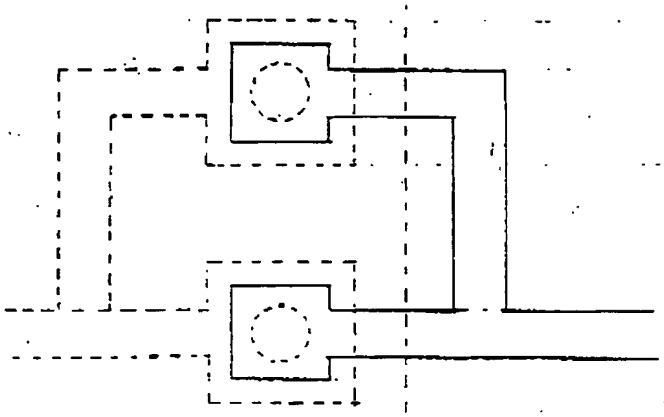
チップスケールパッケージにおいて接合部の線を多重化し接合不良率を低減する構造と工法。

703-10074

7. 【サーチのための国際特許分類・キーワード】

CSP、BGA、チップサイズパッケージ、チップスケールパッケージ H01L、H05K

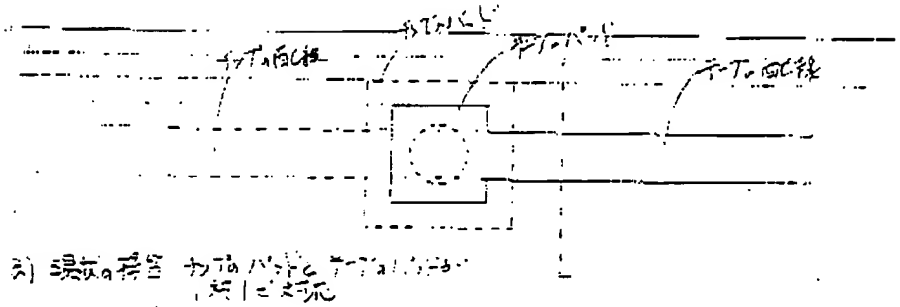
8. 1【発明の図】



(平面図)

b) 改善案 チップとテープの配線を複数にすることで、接合不良による断線の確率を低減できる

8. 2【従来の図】



a) 従来の構造 チップのパッドとテープの配線が1対1で接続

IDEA PROPOSAL

Department Reference No. 753-10074

Proposed date: September 29, 1997

Group code: Internal No.0174

Approved by: Manager, MORISHIGE

Department to which proposer belongs:

Head department of semiconductor high density packaging

Development section of packaging technology

Name of proposer: Shuichi MATSUDA

Field of application: Semiconductor IC packaging

Applied product: CSP

Experiment or Prototype: Experiment

Prior patent (Patent publication number): Non

Prior reference: Non

Superior name: Hirohumi NAKAJIMA

Determination:

Patent application in foreign country: US

Evaluation committee

Name of person in charge of evaluation:

Sueo MORISHIGE, Kenji SUGAWARA

Determined date: October 3, 1997

Result of evaluation: Application

Patent Application in foreign country: US

I have understood contents of the invention by reading one to four pages in the proposal sheet including the drawing

Kenichiro KATA

1. 【Title of the Invention】

Assembly method of semiconductor IC (Integrated Circuit) device (Method for reducing open fault at joint portion by making wiring multiple)

2. 【Feature of the Invention】

In the chip size package in which a carrier tape and a joint electrode with a semiconductor chip formed on the carrier tape is junctioned to an electrode of a chip, a plurality of electrodes of semiconductor chips is mounted for a single wiring and connection is established between them, and a plurality of joint sections corresponding to the chip electrodes for one wiring on a side of a carrier tape is mounted and, by connecting them, the carrier tape and the joint section of the semiconductor chip can have a plurality of paths for one wiring. In many cases, electrical failures in the assembly of the chip size package are attributable to open faults at the joint section. By using a plurality of paths at the joint section, it is possible to lower the occurrence ratio of the open fault.

3.1 【Configurations, operations, manufacturing method and procedures in the Invention】

A plurality of chip electrodes is used for single wiring of power-source / ground line in particular. To correspond to this, a plurality of the joint electrode of the carrier tape is mounted. By connecting them, the single wiring can have a plurality of transmission paths at the joint section between the chip and the tape.

3.2 【Main effects of the Invention】

By making multiple the wiring at the joint section where the failure easily occurs, it is possible to remarkably reduce the open fault. Moreover, places where the wiring is made multiple is the ground / power source line and these lines are placed at the corner portion of the chip in many cases. Since the corner portion is a place where greatest differences in thermal expansion between the chip and the carrier tape occur, the increase in the joint sections at the corner portion serves to dynamically increase the strength between the chip and the carrier tape, thus decreasing the connection fault.

3.3 【Reasons for achievement of above effects】

By making multiple the wiring at the joint section, even if the open fault occurs in one of the paths, conductivity can be obtained by other path. Moreover, by mutual reinforcement among adjacent joint sections, it is possible to withstand the difference in the thermal expansion between the carrier tape and the chip.

4. 【Embodiment of the Invention】

Embodiment of the invention is shown in the attached drawing. In the assembly of the chip size package, a plurality of liens corresponding to the ground wiring is used both on the sides of the tape and the chip and they are junctioned to each other.

4.1 【Configurations in embodiment】

In the joint section made up of the carrier tape and the

chip, for the existing wiring of the chip, additional electrodes having the same potential are mounted. Additional pads having the same potential for the existing pad are also mounted in the chip and each of them is connected.

4.2 【Description of operations in embodiment】

Since the joint section has the two paths for the single wiring, even if the open fault occurs in one of them, a pin outside the package does not become defective. As a result, it is possible to remarkably lower the occurrence rate of the open faults.

4. 3 【Modified embodiment of the Invention】

By adding wiring to the single wiring and having the joint section use three paths, it is possible to more lower the occurrence rate of the open faults.

5.1 【Configurations and operations, manufacturing method, procedures or likes in conventional method】

In the conventional method, a single joint electrode is mounted for the chip using one single wiring and an electrode corresponding the carrier tape is also mounted and they are junctioned by a thermocompression junction method by applying ultrasonic waves and electrical conductivity in the package is obtained from the chip. There is a possibility of the occurrence of connection fault in such the joint sections and defectives are excluded by O/S inspection process or selection process.

5.2 【Main disadvantages in conventional method】

Since the power source and ground lines are operated to function by a plurality of wirings and each of them has the same electric potential, and, for example, if the ground line has 10 pins and one pin has a failure, it is impossible to detect the failure by the present O/S inspection process or selection process. Since this failure is detected for single pin by electrical inspection, it becomes object of claims from the customer.

5.3 【Reason for occurrence of above advantages】

In the present inspection process, the power source lines and ground lines having the same potential, single open fault cannot be detected.

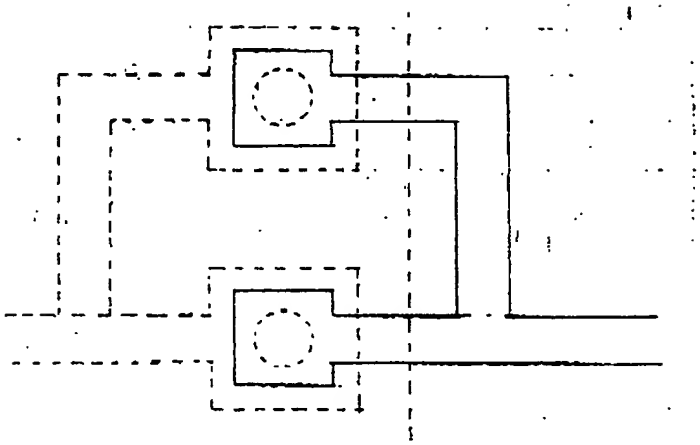
6. 【Scope of right】

Configuations and method for reducing connection fault by multiplexing the joint section in chip scale package.

7. 【IPC for search and keywords】

CSP, BGA, chip size package, chip scale package, H01L, H05K

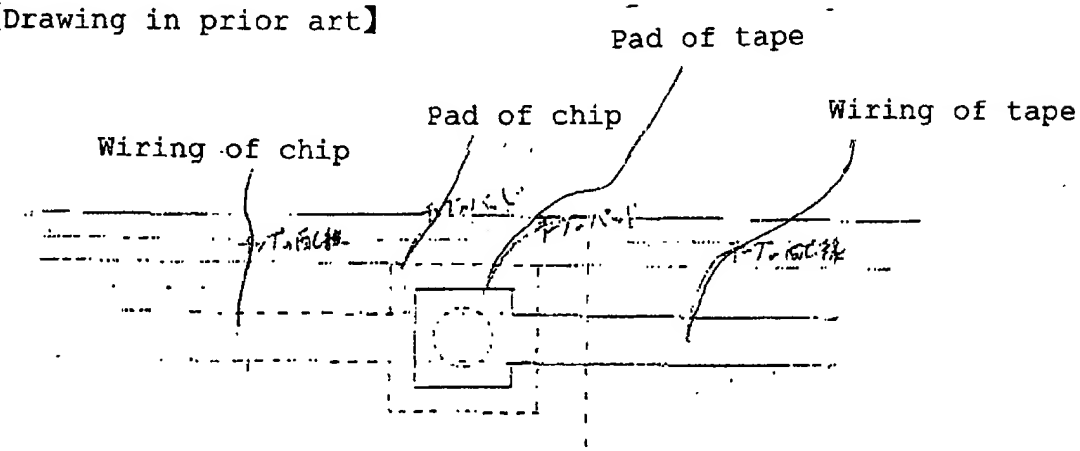
8.1 【Drawing of the Invention】



[Plan View]

b) Measure for improvement: By using a plurality of wirings for the chip and tape, a probability of the disconnection caused by connection fault can be decreased.

8.2 【Drawing in prior art】



b) Junction in conventional method

Pad of chip corresponds to bump of tape in one-to-one manner